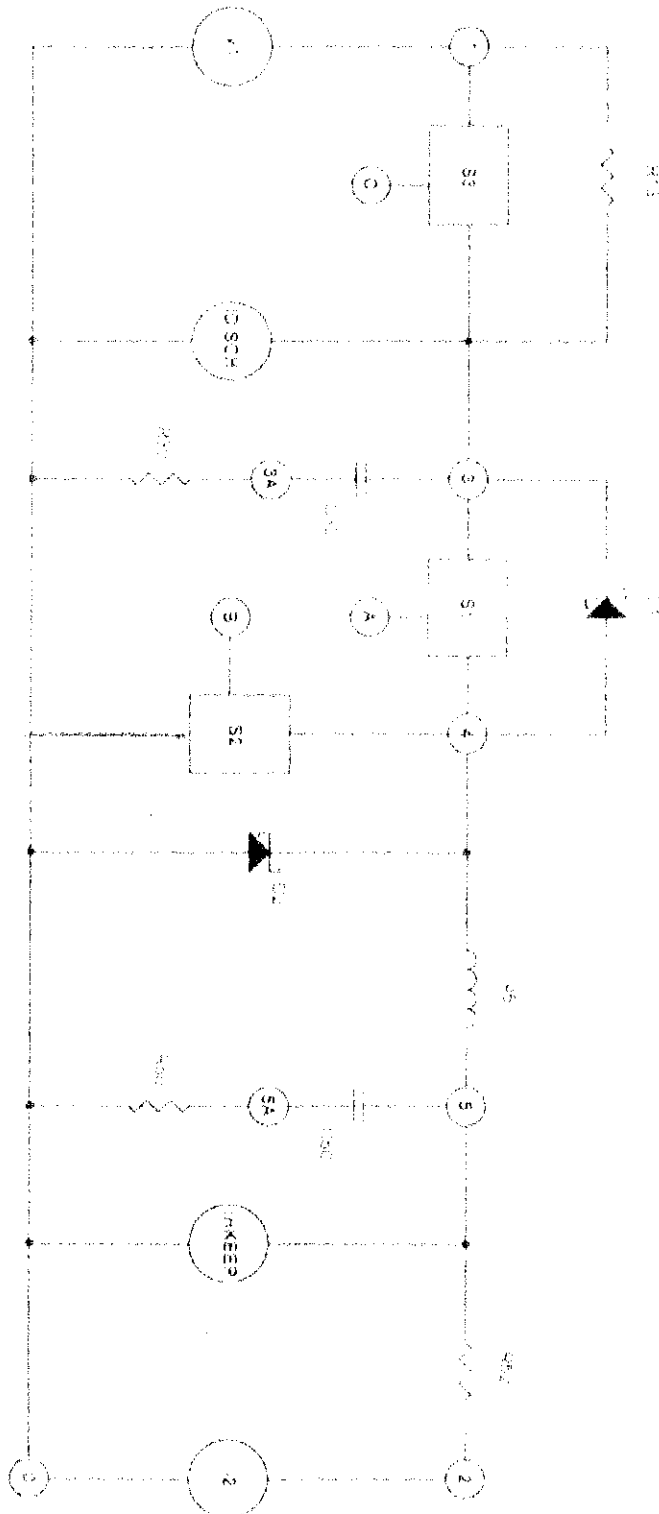


Switching type AC-DC-converter

ATTACHMENT- 8

c) Delphi P-Spice based
Model, Program, and Results



RENPMSPICE
(renpmA.dsn)

*DELPHI P-SPICE
DELTA-1000
DELTA-1000*

RENPWM03.CIR HF PWM Behavioral Model of DC Xfmr
* 500KHZ behavioral simulation of Renault DC Transformer

.TRAN 0.01U 0.5M 0U 0.01U UIC

.PROBE

.WATCH TRAN V(1) V(2) I(R52)

.PARAM VIN = 42.0V

.PARAM ILOAD = 80A

.STEP PARAM ILOAD 0 80 40

.PARAM D = 0.338

V10	1	0	{VIN}	
IDISCH	3	0	0.40A	✓
I20	2	0	{ILOAD}	✓
IHKEEP	5	0	1.09A	
VS1	A	0	PULSE(-1 2	0 {RTS} {OTS} {S1ON} 2U)
VS2	B	0	PULSE(-1 2	{S1ON+0.02U} {RTS} {OTS} {S2ON} 2U)
VS3	C	0	{ILOAD}	
C30	3	0	20.0UF	IC= {VIN}
C50	5	5A	50.0UF	IC= {VIN/3}
L45	4	5	2.00UH	IC= {ILOAD}
R13	1	3	0.0500	
R50	5A	0	0.0500	
R52	5	2	0.0134	
D1	4	3		DMBR3045
D2	0	4		DMBR3045
S1	3	4	A 0	SIFET
S2	4	0	B 0	SIFET
S3	1	3	C 0	SIFET

.PARAM RTS= 0.01U OTS= 0.01U S1ON= {(D*2U)-0.02U}

.PARAM S2ON= {((1-D)*2U)-0.02U}

.MODEL SIFET VSWITCH (RON= 0.001 ROFF= 100K VON= 1 VOFF= 0)

.MODEL DMBR3045 D(IS=489n RS=7.299m IKF=80.79 N=1 EG=1.11

+ XTI=0 CJO=2.144n ISR=7.268u VJ=0.75 M=0.4923 FC=0.5 NR=2)

.OPT ACCT RELTOL=0.005 ABSTOL=1UA VNTOL=0.1MV PIVREL=0.005

.OPT PIVTOL=1E-12 CHGTOL=0.005P GMIN=1E-10

.OPT ITL1=100 ITL2=100 ITL4=100 ITL5=0

.END

John --

Dr. Yilmaz Sahinkaya had several questions about the operation of the DC - DC Converter schematic diagram (of an analytical model) that we sent to him a few weeks ago. This diagram does not reflect the circuit that we are actually using, but its "black box" characteristics are very close. To answer the questions, I'll now proceed to discuss the operation of the circuit in some detail.

DC to DC Converter

The circuit as supplied had a connection that should be made from the bottom of the switch S1 to common (0). I am enclosing a correct schematic. (Please note that the SPICE analysis did include the missing connection.)

The circuit is basically a simple pulse width modulated buck regulator. To this we have added synchronous rectification (thus bidirectionality) and several loss elements (so that the circuits efficiency close to that of the actual circuit).

The main switches are S1 and S2. R13, IDISCH, IHKEEP and R52 are used to create loss and regulation (in the cases of R13 and R52), and S3 is used to introduce the loss of R13 in the backward direction of circuit operation. For the purpose of testing V1 (a 42Vdc source) and I2 (a stepped current load) are included in the demonstration analysis that is provided.

In the forward mode, that is the flow of positive current from node (5) to node (2) (i.e. I2 has a positive sign), the loss added by the flow of current through the resistor R13 is not used. Therefore, S3 is closed. Where that loss and regulation (the circuit runs with fixed duty cycle) is needed for the backward mode, S3 is turned off.

The displacement current losses caused by the voltage changes across the diodes D1 and D2 are too low. Therefore, the loss current sink DISCH is added to help create the proper no load loss. Another source of loss is housekeeping power (the small signal and gate drive losses), this is modeled by the loss current sink IHKEEP. R52 contributes the primary source of load-induced loss and regulation.

R30 and R50 contribute relatively little loss but cause input and output ripple voltage similar to that of the actual circuit. Finally, L45, modeled as a linear element, is chosen to provide transient response like that of the actual circuit.

Other comments:

Perhaps a few more words will help explain some answers in more detail.

The operating frequency (at 500kHz) is very high, the value of L45 (at 2 uH) is so low, and there is no closed loop, that the model circuit's transient response is close to that of the actual circuit. (A short length of harness in the car may be worse.) The actual circuit does not exhibit saturation of its inductors; neither does the model circuit exhibit saturation of L45.

The test demonstration was run only in the forward direction with an input voltage fixed at 42Vdc. The output current was stepped from zero, to 40Adc, to 80Adc (corresponding to no load, approximately one-half rated load, and approximately rated load, respectively). ✓

The efficiency is determined as a computed variable in a transient analysis. The transient aspect is rather meaningless. The values that are approached asymptotically are of significance (0, 92%, and 90% for 0A, 40A, and 80A, respectively). The equation for efficiency is expressed in terms of variables and parameters as follows:

$$\text{Efficiency (in \%)} = 100 * (\text{output power}) / (\text{input power})$$

$$\text{Efficiency (in \%)} = 100 * (\text{output voltage}) * (\text{output current}) / ((\text{input voltage}) * (\text{input current}))$$

$$\text{Efficiency (in \%)} = 100 * (\text{voltage at node (2)}) * (\text{current through resistor R52}) / ((\text{voltage at node (1)}) * (\text{current through switch S3}))$$

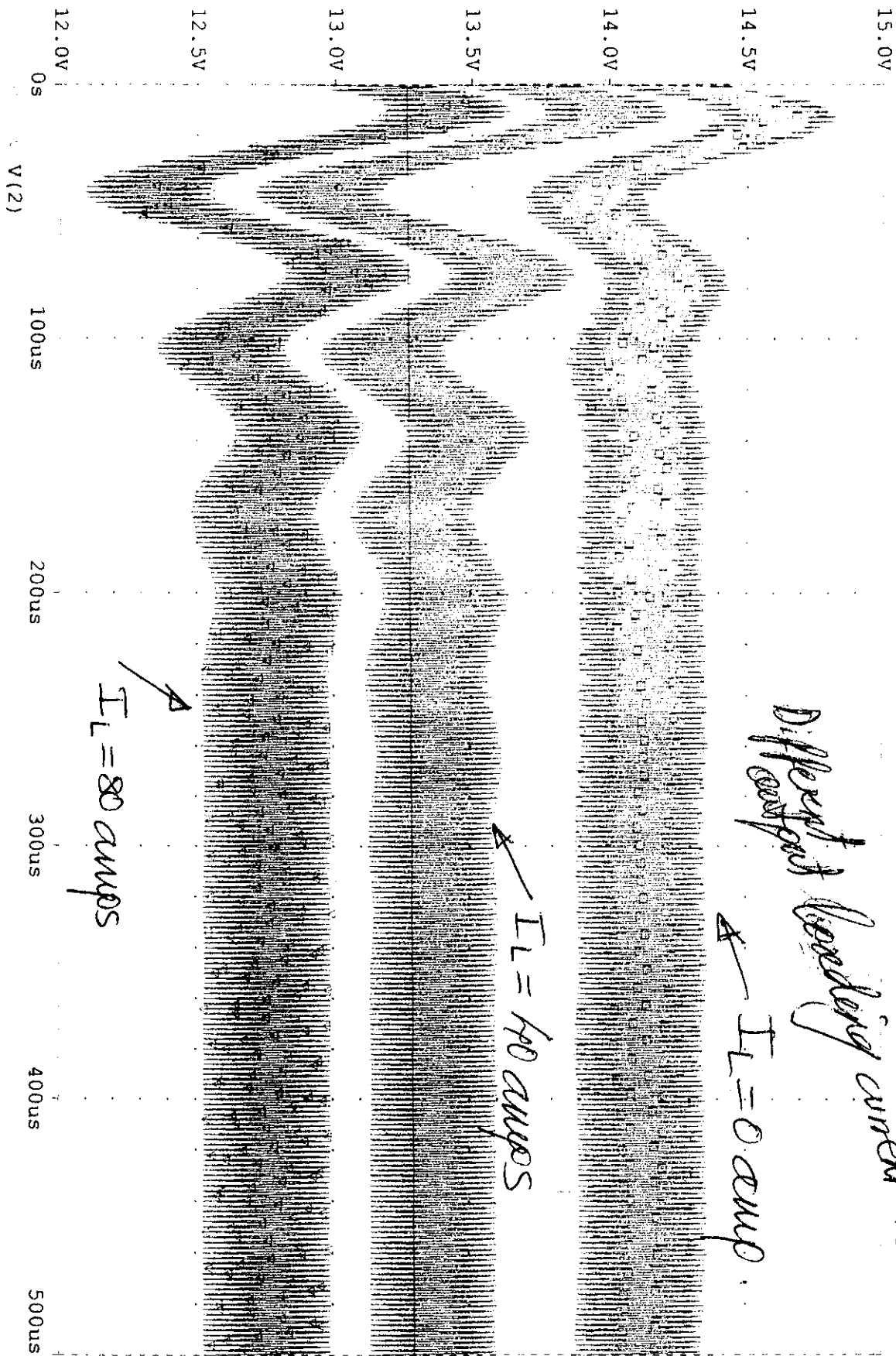
and where avg (meaning average) is used as a filtering function.

Date/Time run: 08/31/99 13:41:10

RENPMW03.CIR HF PWM Behavioral Model of DC Xfmr

Temperature: 27.0

(A) Renpmw03.dat



Date: August 31, 1999

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Time: 14:19:36

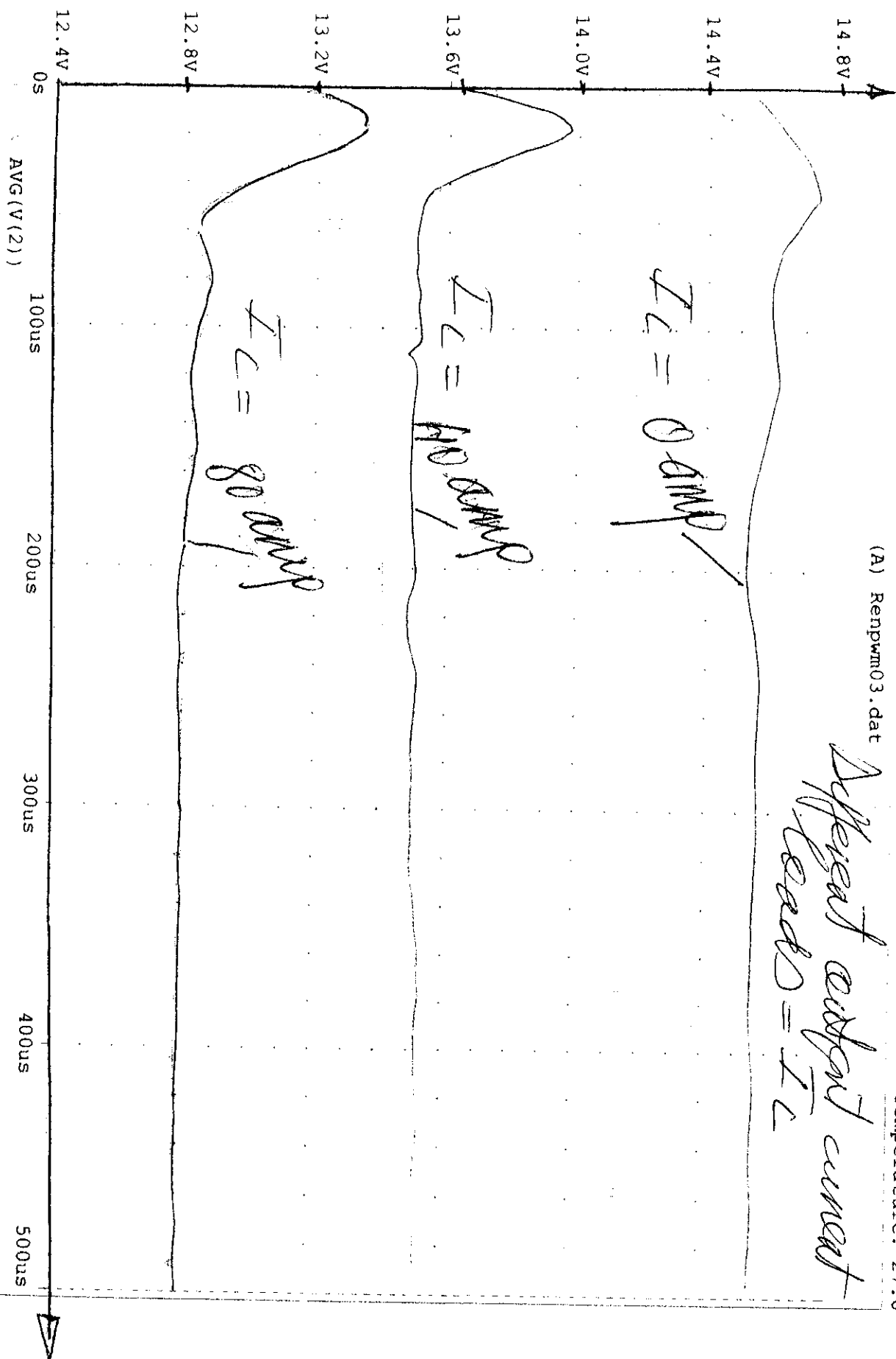
Date/Time run: 08/31/99 13:41:10

RENPMW03.CIR HF PWM Behavioral Model of DC Xfmr

(A) Renpwm03.dat

Temperature: 27.0

*Different output current
loads $I_L = I_C$*



Date: August 31, 1999

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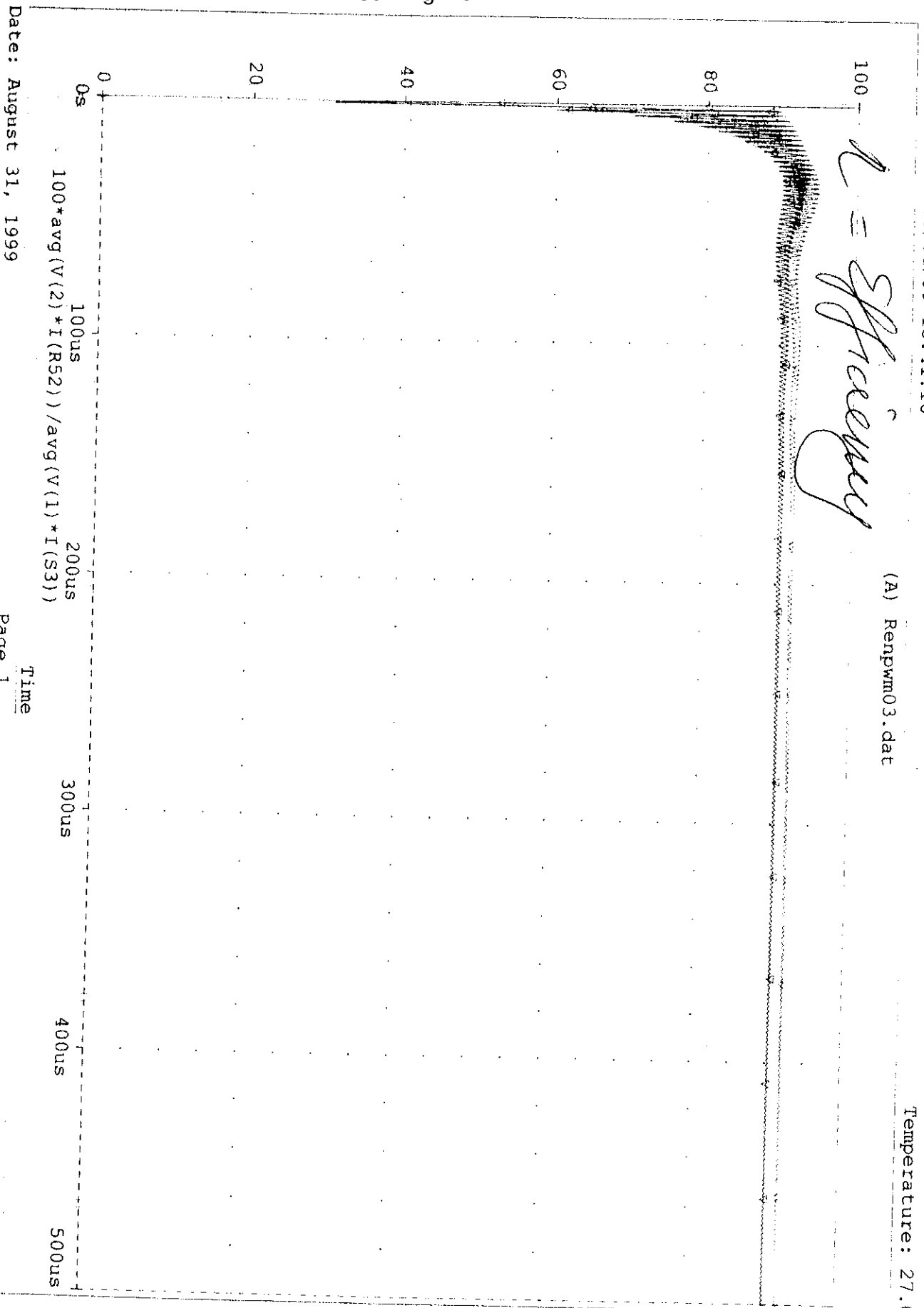
Time: 14:02:20

RENPMW03.CIR HF PWM Behavioral Model of DC Xfmr
Date/Time run: 08/31/99 13:41:10

Temperature: 27.0

Handwritten: $\eta = \text{Efficiency}$

(A) Renpwm03.dat



Date: August 31, 1999

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Time: 14:23:43